CHAPTER 1:
Gallium Nitride (GaN) Technology Overview

Silicon Power MOSFETs from 1976-2010

For over three decades power management efficiency and cost showed steady improvement as innovations in power in power MOSFET (metal oxide silicon field effect transistor) structures, technology, and circuit topologies paced the growing need for electrical power in our daily lives. In the new millennium, however, the rate of improvement slowed as the silicon power MOSFET asymptotically approached its theoretical bounds.

Power MOSFETs first started appearing in 1976 as alternatives to bipolar transistors. These majority carrier devices were faster, more rugged, and had higher current gain than their minority-carrier counterparts. As a result, switching power conversion became a commercial reality. AC-DC switching power supplies for early desktop computers were among the earliest volume consumers of power MOSFETs, followed by variable speed motor drives, fluorescent lights, DC-DC converters, and thousands of other applications that populate our daily lives.

One of the earliest power MOSFETs was the IRF100 from International Rectifier Corporation, introduced in November 1978. It boasted a 100 V drain-source breakdown voltage and a 0.1 Ω on-resistance; the benchmark of the era. With a die size over 40 mm^2, and with a $34 price tag, this product was not destined to broadly replace the venerable bipolar transistor immediately.

Many generations of power MOSFETs have been developed by several manufacturers over the years. Benchmarks were set, and fell, every year or so for 30 plus years. As of the date of this writing, the 100 V benchmark is arguably held by Infineon with the IPB025N10N3G. In comparison with the IRF100's resistivity figure of merit of 4 Ω – mm^2, the IPB025N10N3G has figure of merit of less than 0.1 Ω – mm^2 [1]. That is almost at the theoretical limit for a silicon device [2].

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There are still improvements to be made. For example, superjunction devices and IGBTs have achieved conductivity improvements beyond the theoretical limits of a simple vertical majority carrier MOSFET. These innovations may still continue for quite some time and will certainly be able to leverage the low cost structure of the power MOSFET and the well-educated base of designers who, after many years, have learned to squeeze every ounce of performance out of their power conversions circuits and systems.

The GaN Journey Begins

HEMT (High Electron Mobility Transistor) gallium nitride (GaN) transistors first started appearing in about 2004 with depletion-mode RF transistors made by Eudyna Corporation in Japan. Using GaN on silicon carbide (SiC) substrates, Eudyna successfully brought transistors into production designed for the RF market [3]. The HEMT structure was based on the phenomenon first described in 1975 by T. Mimura et al. [4] and in 1994 by M. A. Khan et al. [5], which demonstrated unusually high electron mobility described as a two-dimensional electron gas (2DEG) near the interface between an AlGaN and GaN heterostructure interface. Adapting this phenomenon to gallium nitride grown on silicon carbide, Eudyna was able to produce benchmark power gain in the multi-gigahertz frequency range. In 2005, Nitronex Corporation introduced the first depletion mode radio frequency (RF) HEMT transistor made with GaN grown on silicon wafers using their SIGANTIC® technology [6].

GaN RF transistors have continued to make inroads in RF applications as several other companies have entered in the market. Acceptance outside this market, however, has been limited by device cost as well as the inconvenience of depletion-mode operation.

In June 2009 Efficient Power Conversion Corporation (EPC) introduced the first enhancement-mode gallium nitride on silicon (eGaN) field effect transistor (FET) designed specifically as power MOSFET replacements. These products were to be produced in high-volume at low cost using standard silicon manufacturing technology and facilities.

The basic requirements for power semiconductors are efficiency, reliability, controllability, and cost effectiveness. Without these attributes, a new device structure would have no chance of economic viability. There have been many new structures and materials considered as a successor to silicon; some have been economic successes, others have seen limited or niche acceptance. In the next section we will look at the comparison between silicon, silicon carbide, and gallium nitride as candidates for the dominant platform for next-generation power transistors.

Why Gallium Nitride?

Silicon has been a dominant material for power management since the late 1950's. The advantages silicon had over earlier semiconductors such as germanium or selenium could be expressed in four key categories:

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- Silicon enabled new applications not possible in earlier materials
- Silicon proved more reliable
- Silicon was in many ways easier to use
- Silicon devices were lower cost

All of these advantages stemmed from the basic physical properties of silicon combined with a huge investment in manufacturing infrastructure and engineering. Let's look at some of those basic properties and compare them with other successor candidates. Table 1.1 shows four key electrical properties of three semiconductor materials contending for the power management market.

Properties*	GaN	Si	SiC
E_G (eV)	3.4	1.12	3.2
E_{BR} (MV/cm)	3.3	0.3	3.5
V_S (x 10^7 cm/s)	2.5	1.0	2.0
μ (cm^2/Vs)	990 - 2000	1500	650

Table 1.1: Material properties of GaN, SiC, and silicon at 300 Kelvin [7,8,9,10,11]

One way of translating these basic crystal parameters into a comparison of device performance in a power transistor is to calculate the best theoretical performance that could be achieved in each of the three candidates. For power devices there are many characteristics that matter in the variety of power conversion systems available today. Five of the most important characteristics are conduction efficiency, breakdown voltage, switching efficiency, size and cost.

Using the data from table 1.1 (and adjusting for the enhanced mobility of the GaN 2DEG), we can calculate the theoretical minimum device on-resistance (the inverse of conductivity) as a function of breakdown voltage and as a function of material [8].

As shown in figure 1.1, SiC and GaN both have a superior relationship between on-resistance and breakdown voltage due to their higher critical electric field strength. This allows devices to be smaller and the electrical terminals closer together for a given breakdown voltage requirement. GaN has an extra advantage compared with SiC as a result of the enhanced mobility of electrons in the 2DEG. This translates into a GaN device with a smaller size for a given on-resistance and breakdown voltage.

*E_G is the bandgap energy, E_{BR} is the critical electric field for breakdown in the crystal, V_S is the saturated drift velocity, and μ is the mobility of electrons. Gallium Nitride gains an additional boost to the mobility (μ) by virtue of the ability to form a 2DEG at the GaN/AlGaN interface. This 2DEG more than doubles the mobility of electrons (from 990 cm^2/Vs to about 2000 cm^2/Vs [7]).

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In figure 1.2 is a comparison between silicon MOSFET and eGaN FET power losses for a common buck converter circuit (discussed in detail in chapter 5). The on-resistances of the transistors are equal, so the difference in total power losses can be attributed to the superior switching capability of the eGaN FETs. The improved switching losses are also discussed in more general terms in chapter 2.

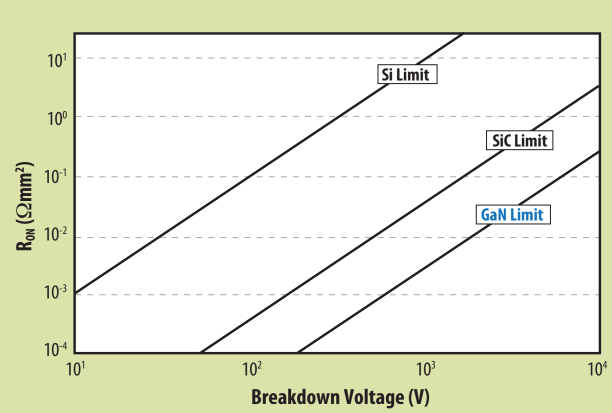

Figure 1.1: Theoretical on-resistance vs blocking voltage capability for silicon, silicon-carbide, and gallium nitride [9].

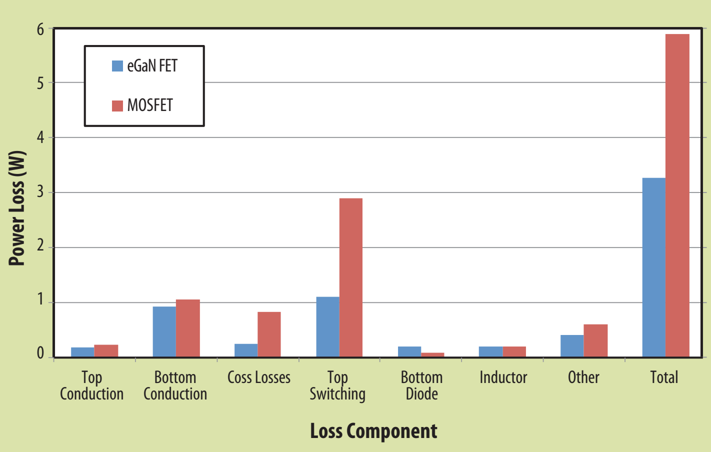

Figure 1.2: Comparison of switching losses of eGaN FETs vs silicon MOSFETs in a 12 V-1.2 V buck converter operating at 1MHz. For each socket both devices have similar $R_{DS(ON)}$.

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Table 1.2 is a comparison of the size of the eGaN FETs compared with equivalent on-resistance MOSFETs. The double advantage of the efficient chipscale LGA package and the smaller die size translate into a significant reduction on overall size occupied by the eGaN FET on a printed circuit board (PCB).

Device	LGA Package	Equivalent MOSFET Packages		
40 V 4 mΩ max	4.1 x 1.6 mm	5 x 6mm PQFN	6.3 x 5 mm DirectFET	5 x 6 mm PolarPak
40 V 16 mΩ max	1.7 x 1.1 mm		4.8 x 3.9 mm DirectFET	
100 V 7 mΩ max	4.1 x 1.6 mm			
100 V 30 mΩ max	1.7 x 1.1 mm		4.8 x 3.9 mm DirectFET	
2000 V 100 mΩ max	1.7 x 0.9 mm		6.3 x 5 mm DirectFET	5 x 6 mm PolarPak

Table 1.2: Comparison between power MOSFETs in various packages and eGaN FETs in LGA packages

eGaN FETs stem from a relatively new technology and, as such, remain somewhat more expensive to produce than their silicon counterparts. This, however, is a temporary situation. As we will discuss in detail in chapter 14, there are no insurmountable barriers to achieving an even lower cost for an equivalent performance eGaN FET compared with a power MOSFET or IGBT.

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Basic GaN FET Structure

The basic GaN transistor structure is shown in figure 1.3. As with any power FET, there are gate, source, and a drain electrodes. The source and drain electrodes pierce through the top AlGaN layer to form an ohmic contact with the underlying 2DEG. This creates a short-circuit between the source and the drain until the 2DEG "pool" of electrons is depleted and the semi-insulating GaN crystal can block the flow of current. In order to deplete the 2DEG, a gate electrode is placed on top of the AlGaN layer. In many of the early GaN transistors, this gate electrode was formed as a Schottky contact to the top surface. By applying negative voltage to this contact, the Schottky barrier becomes reverse biased and the electrons underneath are depleted. Therefore, in order to turn this device OFF, a negative voltage relative to both drain and source electrodes is needed. This type of transistor is called a depletion mode, or d-mode, Heterostructure Field Effect Transistors (HFET).

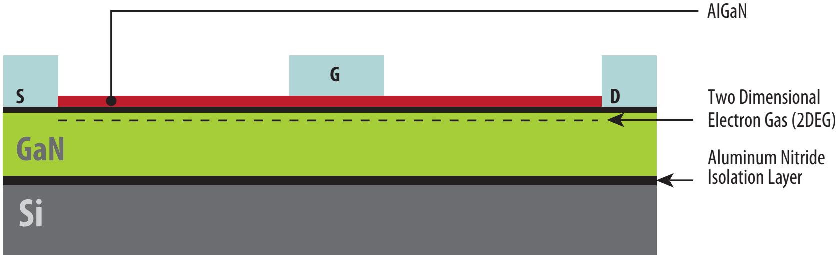

Figure 1.3: Typical AlGaN/GaN HFET structure with three metal-semiconductor contacts for the source, gate and drain.

In power conversion applications, d-mode devices are inconvenient because, at the startup of a power converter, a negative bias must first be applied to the power devices or a short-circuit will result. An enhancement mode (e-mode) device, on the other hand, would not suffer this limitation. With zero bias on the gate, an e-mode device is OFF and will not conduct current. A comparison of output characteristics between a d-mode and e-mode FET are shown in figure 1.4. When Efficient Power Conversion Corporation introduced the first commercial enhancement mode gallium nitride FETs, it significantly reduced the level of difficulty designing power conversion systems with GaN transistors.

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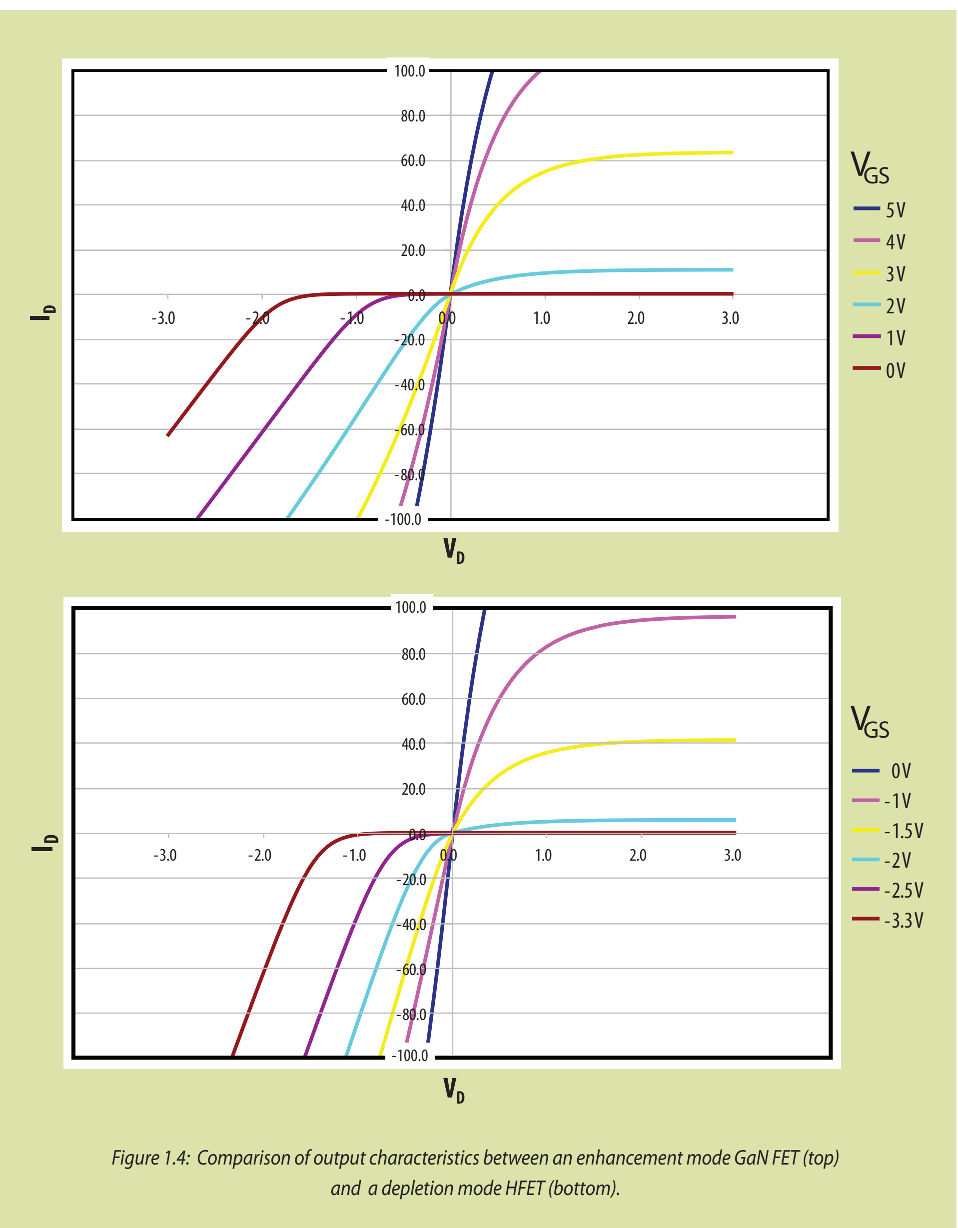

Figure 1.4: Comparison of output characteristics between an enhancement mode GaN FET (top) and a depletion mode HFET (bottom).

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eGaN® FET Structure - Enhancement Mode

EPC's enhancement mode process begins with silicon wafers. A thin layer of Aluminum Nitride (AlN) is grown on the silicon to provide a seed layer for the subsequent growth of a gallium nitride heterostructure. A heterostructure of aluminum gallium nitride (AlGaN) and then GaN is grown on the AlN. This layer provides a foundation on which to build the eGaN FET. A very thin AlGaN layer is then grown on top of the highly resistive GaN. It is this thin layer that creates a strained interface between the GaN and AlGaN crystals layers. This interface, combined with the intrinsic piezoelectric nature of GaN, creates a 2DEG which is filled with highly mobile and abundant electrons [10]. Further processing of a gate electrode forms a depletion region under the gate. To enhance the FET, a positive voltage is applied to the gate in the same manner as turning on an n-channel, enhancement mode power MOSFET. A cross section of this structure is depicted in figure 1.5. Additional layers of metal are added to route the electrons to gate, drain, and source terminals (see figure 1.6 cross section). This structure is repeated many times to form a power device as shown in figure 1.7. Conveniently, eGaN FETs behave similarly to silicon MOSFETs with some exceptions that will be explained in the following sections.

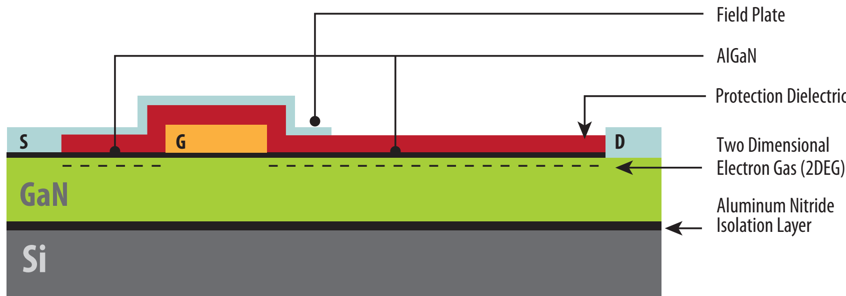

Figure 1.5: eGaN FET structure.

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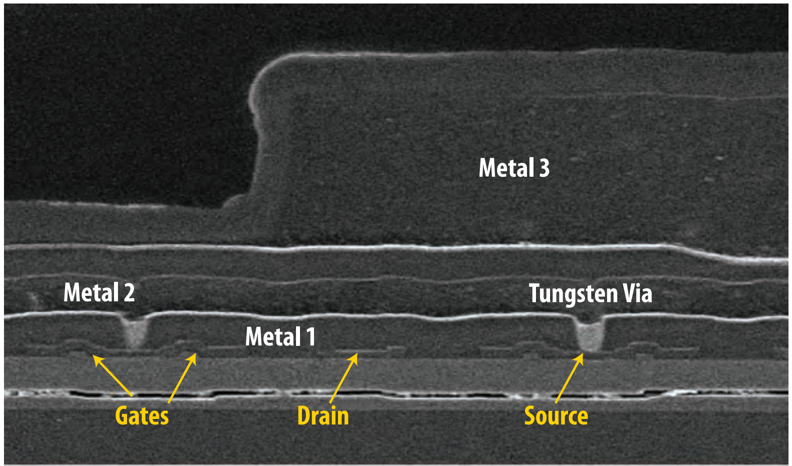

Figure 1.6: SEM micrograph of an eGaN FET.

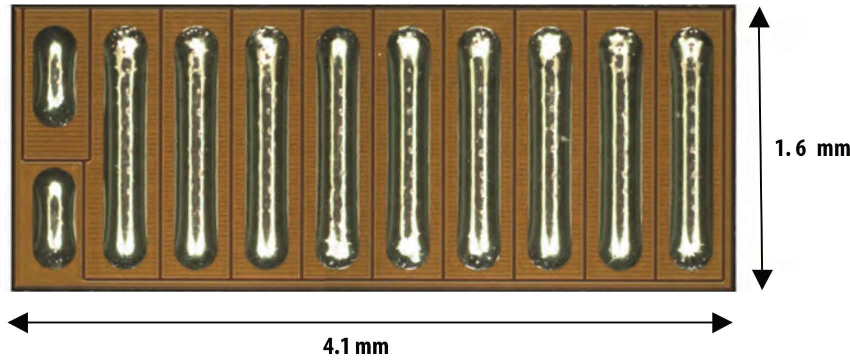

Figure 1.7: Top view of a completed eGaN FET. This device is rated at 40 V, 4 mΩ, and 33 A.

eGaN® FET Basic Electrical Characteristics

On-Resistance

On-resistance ($R_{DS(ON)}$) versus gate-source voltage (V_{GS}) curves are similar to MOSFETs. EPC first generation GaN transistors are designed to operate with a 4-5 V gate drive. The temperature coefficient of $R_{DS(ON)}$ of the eGaN FET is also similar to the silicon MOSFET as it is positive, but the magnitude is significantly less. At 125°C the $R_{DS(ON)}$ is 1.45 times the $R_{DS(ON)}$ at 25°C for the EPC1001 compared to 1.7 for silicon. This advantage increases with increasing device voltage rating.

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Gate Threshold Voltage

The threshold of eGaN FETs is lower than that of silicon MOSFETs. This is made possible by the almost flat relationship between threshold and temperature along with the very low gate-to-drain capacitance (C_{GD}) as described later in this chapter. Since the device starts to conduct significant current at 1.6 V, care must be taken to ensure a low impedance path from gate to source when the device needs to be held off during high speed switching in a rectifier function.

Capacitance

In addition to the low $R_{DS(ON)}$, the lateral structure of the eGaN FET makes it a very low capacitance device as well. It has the capability of switching hundreds of volts in nanoseconds, giving it multiple megahertz capability. Most important in switching is C_{GD}. With the lateral structure, C_{GD} comes only from a small corner of the gate and is much lower than the same capacitance in a vertical MOSFET.

Gate-to-source capacitance (C_{GS}) consists of the junction from the gate to the channel, and the capacitance of the dielectric between the gate and the field plate. C_{GS} is large when compared with C_{GD}, giving eGaN FETs good dv/dt immunity, but still small when compared with silicon MOSFETs. This results in very short delay times, and good controllability in low duty cycle applications (e.g. A 48 V to 1 V buck regulator has been demonstrated at 1 MHz using 100 V eGaN FETs from EPC [12] and is discussed in chapter 5.) The drain-to-source capacitance CDS is also small, being limited to the capacitance across the dielectric from the field plate to the drain. Capacitance versus Voltage curves for eGaN FETs are similar to those for silicon except that, for a similar resistance, its capacitance is significantly lower.

Body Diode

The last part of the performance picture is that of the so-called "body diode." As seen from figure 1.5, EPC's GaN transistor structure is a purely lateral device, absent of the parasitic bipolar junction common to silicon-based MOSFETs. As such, reverse bias or "diode" operation has a different mechanism but similar function. With zero bias gate to source there is an absence of electrons under the gate region. As the drain voltage is decreased, a positive bias on the gate is created relative to the drift region, injecting electrons under the gate. Once the gate threshold is reached, there will be sufficient electrons under the gate to form a conductive channel. The benefit to this mechanism is that there are no minority carriers involved in conduction, and therefore no reverse recovery losses. While Q_{RR} is zero, output capacitance (C_{OSS}) has to be charged and discharged with every switching cycle. For devices of similar $R_{DS(ON)}$, eGaN FETs have significantly lower C_{OSS} than silicon MOSFETs. As it takes a bias on the gate greater than the threshold voltage to turn on the eGaN FET in the reverse direction, the forward voltage of the "diode" is higher than silicon transistors.

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Since the fundamental operation of eGaN FETs is similar to that of silicon MOSFETs, they can be represented schematically the same way as shown in figure 1.8.

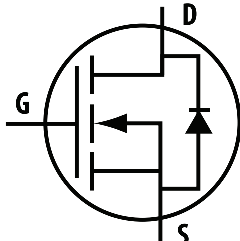

Figure 1.8: Standard symbol for an enhancement mode MOSFET or eGaN FET.

Summary

In this chapter we introduced a new technology for making power transistors using gallium nitride grown on top of silicon. Enhancement mode transistors have characteristics very similar to the power MOSFET, but with improved high speed switching, lower on-resistance, and a smaller size than their silicon predecessors. These new capabilities, married with a step forward in high-density packaging, enable power conversion designers to reduce power losses, reduce system size, improve efficiency, and ultimately, reduce system costs.

Chapter 2 describes the electrical and thermal properties in greater detail and compares these properties with state-of-the-art MOSFETs.

Chapters 3 and 4 go into detail about the techniques for circuit design and board layout in order to lay a foundation for the applications examples given in chapters 5 through 8. Each of these applications examples demonstrates the ability of eGaN FETs to significantly improve power conversion efficiency.

In chapter 9 is discussed how best to use the SPICE models to simulate circuits using eGaN FETs, and in Chapter 10 we describe how to assemble the land grid array (LGA) package format for a reliable end-product.

Chapters 12 and 13 are about the reliability of eGaN FETs under various environmental stresses including high voltage, high temperature, high humidity, and even high radiation.

Finally, in chapter 14 is discussed the "why, when, and how" eGaN FETs will displace MOSFETs over the coming years.

These are the early years of a great new technology.

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